CLAIMS

We claim:

1. An arrangement comprising a first semiconductor chip and a second semiconductor chip connected thereto,

- where the second semiconductor chip is additionally connected to electrical loads and drives these electrical loads on the basis of a timing which is defined by load control data,
- where the first semiconductor chip transmits to the second semiconductor chip the load control data and pilot data which control the second semiconductor chip, and
- where the second semiconductor chip transmits to the first semiconductor chip diagnostic data which represent at least one of states prevailing in the second semiconductor chip and events which occur in the second semiconductor chip,

wherein

the first semiconductor chip includes means for transmitting appropriate pilot data to the second semiconductor chip, and the second semiconductor chip includes means for controlling a transmission rate by which the diagnostic data is transmitted to the first semiconductor chip in accordance with the appropriate pilot data.

2. The arrangement as claimed in claim 1, wherein the first semiconductor chip is a program-controlled unit.

3. The arrangement as claimed in claim 1 wherein the second semiconductor chip is a power chip.

4. The arrangement as claimed in claim 1, wherein
the diagnostic data are transmitted in time with a transmission clock signal generated in the second semiconductor chip, and wherein this transmission clock signal is not transmitted to the first semiconductor chip.

5. The arrangement as claimed in claim 1, wherein
the transmission rate is prescribed by transmitting a division factor, and wherein the second semiconductor chip divides the frequency of a transmission clock signal transmitted to it by the first semiconductor chip by the division factor and transmits the diagnostic data to the first semiconductor chip in time with the resultant transmission signal.

6. The arrangement as claimed in claim 5, wherein
the transmission clock signal supplied to the second semiconductor chip represents the transmission clock which is used by the first semiconductor chip to transmit the load control data or the pilot data to the second semiconductor chip.

7. The arrangement as claimed in claim 6, wherein
the diagnostic data are transmitted in units of frames, where a frame starts with a start bit having a prescribed value and ends with one or two stop bits having prescribed values.

8. The arrangement as claimed in claim 1, wherein the first semiconductor chip ascertains the phase of the diagnostic data by oversampling the diagnostic data.

9. The arrangement as claimed in claim 1, wherein the diagnostic data are transmitted via a line via which neither load control data nor pilot data are transmitted.

10. The arrangement as claimed in claim 1, wherein the load control data and the pilot data are transmitted via a second transmission channel.

11. The arrangement as claimed in claim 10, wherein the second transmission channel comprises

- a transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip,
- a data line via which the first semiconductor chip transmits the load control data and the pilot data to the second semiconductor chip in time with the transmission clock signal, and
- a chip select line via which the first semiconductor chip transmits the chip select signal to the second semiconductor chip, said chip select signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second

semiconductor chip via the data line.

12. The arrangement as claimed in claim 1, wherein
the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing.

13. The arrangement as claimed in claim 12, wherein
the first semiconductor chip defines time windows of constant length and transmits in each time window either a load control data frame or a control data frame or no data.

14. The arrangement as claimed in claim 13, wherein
the first semiconductor chip transmits no further load control data frame for a respective length of n time windows after transmission of a load control data frame, where $n \geq 0$ and where n can be set by the user of the arrangement.

15. The arrangement as claimed in claim 14, wherein
a pilot data frame can be transmitted only in a time window in which no load control data frame is to be transmitted.

16. The arrangement as claimed in claim 13 or 14, wherein
transmission of the pilot data has priority when load control data and pilot data are awaiting transmission simultaneously.

17. The arrangement as claimed in claim 10, wherein the second transmission channel comprises

- a first transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip,
- a second transmission clock line via which the first semiconductor chip transmits the inverse transmission clock signal to the second semiconductor chip,
- a first data line via which the first semiconductor chip transmits the load control data and the pilot data to the second semiconductor chip in time with the transmission clock signal,
- a second data line via which the first semiconductor chip transmits the inverse load control data and the inverse pilot data to the second semiconductor chip, and
- a chip select line via which the first semiconductor chip transmits a chip select signal to the second semiconductor chip, said chip select signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second semiconductor chip via the data line.

18. The arrangement as claimed in claim 17, wherein the output drivers on the first semiconductor chip, which output the load control data, the pilot data and the transmission clock signal, are LVDS drivers or other special drivers whose use allows electromagnetic interference to be kept down.

19. The arrangement as claimed in claim 1, wherein
the first semiconductor chip has a plurality of respective different output drivers for outputting the load control data, the pilot data and the transmission clock signal, and wherein the first semiconductor chip can have prescribed to it which of the plurality of different output drivers needs to be used in each case.